CHAPTER 8

Programmable timer/counter

The Intel 8254

The PCL-818L provides an Intel 8254 programmable interval timer/counter, version 2. The popular 8254 offers three independent 16-bit down counters. Each counter has a clock input, control gate and an output. You can program each counter for maximum count values from 2 to 65535.

Version 2 of the 8254 has a maximum input clock frequency of 10 MHz. The PCL-818L provides 1 MHz and 10 MHz input frequencies to the 8254 from an on-board crystal oscillator. Jumper JP2 controls the input frequency. See Chapter 2 for more information.

Counters 1 and 2 on the 8254 are cascaded and operated in a fixed divider configuration. Counter 1 input connects to the 1 MHz or 10 MHz clock frequency, and the output of Counter 1 connects to the input of Counter 2. The output of Counter 2 is internally configured to provide trigger pulses to the A/D converter, but you can also access it for your own use from connector CN3 pin 37. Counter 0 is not used by the PCL-818L and is available for your use. You can access it through CN3 pin 18.

Counter read/write and control registers

The 8254 programmable interval timer uses four registers at addresses BASE+12, BASE+13, BASE+14 and BASE+15. Register functions appear below:

Register	Function
BASE+12	Counter 0 read/write
BASE+13	Counter 1 read/write
BASE+14	Counter 2 read/write
BASE+15	Counter control word

Since the 8254 counter uses a 16 bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

BASE + 15 – 8254 control, standard mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1 & SC0 Select counter.

Counter	SC1	SC0
0	0	0
1	0	1
2	1	0
Read-back command	1	1

RW1 & RW0 Select read/write operation

Operation	RW1	RW0
Counter latch	0	0
Read/write LSB	0	1
Read/write MSB	1	0
Read/write LSB first, then MSB	1	1

M2, M1 & M0 Select operating mode

M2	M1	M0	Mode
0	0	0	0 interrupt on terminal count
0	0	1	1 programmable one shot
X	1	0	2 Rate generator
X	1	1	3 Square wave rate generator
1	0	0	4 Software triggered strobe
1	0	1	5 Hardware triggered strobe

BCD Select binary or BCD counting.

BCD	Type
0	Binary counting 16-bits
1	Binary coded decimal (BCD) counting

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from 0 to 9999.

If you set both SC1 and SC0 bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

BASE+15 – 8254 control, read-back mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	1	1	CNT	STA	C2	C1	C0	X

CNT = 0 Latch count of selected counter(s).

STA = 0 Latch status of selected counter(s).

C2, C1 & C0 Select counter for a read-back operation.

C2 = 1 select Counter 2

C1 = 1 select Counter 1

C0 = 1 select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:

BASE + 12/13/14 – status read-back mode								
Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	OUT	NC	RW1	RW0	M2	M1	M0	BCD

OUT Current state of counter output

NC Null count is 1 when the last count written to the counter register has been loaded into the counting element

The counter enable register, located at address BASE+10, has a close relationship with the counter operation. Refer to Chapter 4, *Timer/ counter enable register*, for the register data format. The TC0 bit enables and disables the pacer. If TC0 = 0, the pacer is enabled. If TC0 = 1, the pacer is disabled and trigger pulses from the pacer are kept from the A/D until TRIG0 is taken high. The TC1 bit controls the input source for Counter 0. If TC1 = 0, Counter 0 is configured to accept external clock pulses. If TC1 = 1, Counter 0 is internally connected to the 100 KHz clock source.

Counter operating modes

MODE 0 – Stop on terminal count

The output will be initially low after this mode of operation is set. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:

1. Writing to the first byte stops the current counting.
2. Writing to the second byte starts the new count.

MODE 1 – Programmable one-shot

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

MODE 2 – Rate generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register is loaded. You can also synchronize the output by software.

MODE 3 – Square wave generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until timeout, then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 – software triggered strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5 – Hardware triggered strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

Counter operations

Read/write operation

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register (BASE+15).

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 & SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read/load MSB and read/load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

Counter read-back command

The 8254 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. Format is as shown at the beginning of the chapter.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.

Counter latch operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter, then reading the value.

The 8254 supports the counter latch operation in two ways. The first way is to set bits RW1 and RW0 to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

Counter applications

The 8254 programmable interval timer/counter on your PCL-818L interface card is a very useful device. You can program counters 1 and 2 to serve as a pacer to generate A/D conversion trigger pulses. Counter 0 is not committed to any internal use. You can configure it for any supported function; e.g., a square wave generator.